Computer Architecture

Sheet (4)

1 Why is the Wait-for-Memory-Function-Completed step needed when reading from or writing to the main memory?

2 A processor uses a control sequence similar to that in Figure 7.6. Assume that a memory read or write operation takes the same time as one internal processor step and that both the processor and the memory are controlled by the same clock. Estimate the execution time of this sequence.

3 Repeat Problem 7.2 for a machine in which the memory access time is equal to twice the processor clock period.

4 Assume that propagation delays along the bus and through the ALU of Figure 7.1 are 0.3 and 2 ns, respectively. The setup time for the registers is 0.2 ns, and the hold time is 0. What is the minimum clock period needed?

5 Write the sequence of control steps required for the bus structure in Figure 7.1 for each of the following instructions:

(*a*) Add the (immediate) number NUM to register R1.

(*b*) Add the contents of memory location NUM to register R1.

(*c*) Add the contents of the memory location whose address is at memory location NUM to register R1.

Assume that each instruction consists of two words. The first word specifies the operation and the addressing mode, and the second word contains the number NUM.

6 The three instructions in Problem 7.5 have many common control steps. However, some of these control steps occur at different counts of the control step counter. Suggest a scheme that exploits these common steps to reduce the complexity of the encoder block in Figure 7.11.

7 Consider the Add instruction that has the control sequence given in Figure 7.6. The processor is driven by a continuously running clock, such that each control step is 2 ns in duration. How long will the processor have to wait in steps 2 and 5, assuming that a memory read operation takes 16 ns to complete? What percentage of time is the processor idle during execution of this instruction?